R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR CLAIM AMENDMENTS

Support for newly presented claim 24 can be found on page 6, lines 19-21 and page 8, lines 29-32. No new matter has been added.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claim 14 under 35 U.S.C. §112, second paragraph, has been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §102(b)

The rejection of claims 1-5 and 15 under 35 U.S.C. §102 as being anticipated by Yifrach '320 has been obviated by appropriate amendment and should be withdrawn.

Yifrach discloses a TV receiver and buffer system (Title). In contrast, claim 1 of the present invention provides a time-shifted video method comprising delivering real-time video frames and time-shifted video frames for display. The real-time video frames and the time-shifted video frames are generated in

response to a digital input signal. A real-time frame is paused in a transition from the real-time mode to the time-shifted mode. Yifrach is silent regarding pausing the real-time frame during a transition and generating the real-time video frames and the time-shifted video frames in response to a digital input signal. Yifrach fails to disclose or suggest the presently claimed invention and the rejection should be withdrawn.

In particular, the so-called real time path in Yifrach appears to be generated in response to an antenna, not a digital input signal as in presently pending claim 23. While the so-called delayed path of Yifrach discloses a digitizer 21, the non-delayed path is not generated in response to the output of the digitizer 21. Yifrach does not disclose or suggest a digital input signal as presently claimed. As such, claim 23 is fully patentable over Yifrach and the rejection should be withdrawn.

Regarding newly presented claim 23, Yifrach does not disclose or suggest (i) a frame buffer configured to generate a first signal in response to a digital input signal or (ii) an encoder configured to generate a second signal in response to the digital input signal. As such, claim 22 is fully patentable over Yifrach.

Regarding newly presented claim 24, Yifrach does not disclose a transition that is seamless to a viewer. As such, claim 24 is fully patentable over Yifrach.

Regarding claims 20, 21 and 22, Yifrach does not disclose or suggest a time-shifted decoder and a controller as presently claimed. Furthermore, claim 20 provides a time-shifted decoder and a real time decoder. Yifrach is silent regarding a real time decoder and a time-shifted decoder. As such, claims 20, 21 and 22 are fully patentable over Yifrach and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 7-10, 13, 14, 16-18 and 20-21 under 35 U.S.C. §103 as being unpatentable over Yifrach '320 has been obviated by appropriate amendment and should be withdrawn. Claims 7-10, 13, 14 and 16-18 depend, either directly or indirectly, from the independent claims, which are now believed to be allowable.

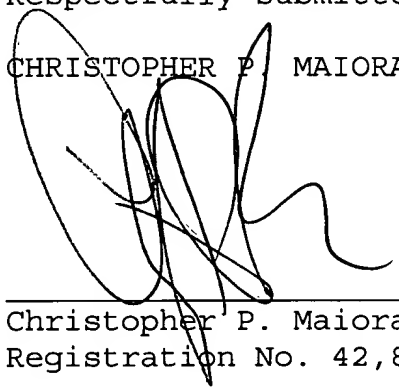
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



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MARKINGS TO SHOW CHANGES MADE

Please replace the paragraph beginning at page 4, line 18 with the following paragraph:

Figure 7 is a block diagram of a single-chip [single-ship] configuration.

Please replace the paragraph beginning at page 9, line 29 with the following paragraph:

As seen in figure 7, such a single chip codec 108, when combined with a common memory 106, may be used to implement a time-shifted system 100 that can handle both incoming compressed and incoming uncompressed video signals 104, 102. Memory 106 serves the functions of both of the buffers 80, 88 of figure 6 [5]. The resulting digital video output 111 is controlled by the host controller to be either real-time or time-shifted as needed.

VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (AMENDED) A time-shifted video method comprising:

in a real-time mode, delivering real-time video frames for display in response to a digital input signal,

in a time-shifted mode, delivering time-shifted video frames for display in response to a digital input signal, the time-shifted video frames being delayed relative to the real-time video frames, and

pausing a real-time frame [in] during a transition from the real-time mode to the time-shifted mode.

2. (AMENDED) The method of claim 1, wherein [in which] the transition is between the paused real-time frame and a time-shifted version of the paused real-time frame.

3. (AMENDED) The method of claim 1, further comprising providing trick functions during the time-shifted mode.

4. (AMENDED) The method of claim 1, wherein [in which] the transition mode is triggered by a command of a viewer or an event generated by software.

5. (AMENDED) The method of claim 1, wherein [in which] the real-time video frames are derived from [input] uncompressed video.

6. (AMENDED) The method of claim 5, wherein [in which] the real-time video frames are provided from an input frame buffer.

7. (AMENDED) The method of claim 1, wherein [in which] the real-time video frames are derived from input compressed video.

8. (AMENDED) The method of claim 7, wherein [in which] the real-time frames are provided from a decoder that decompresses the input compressed video.

9. (AMENDED) The method of claim 1, wherein [in which] the real-time mode, the time-shifted mode, and the transition are provided by a single codec chip.

10. (AMENDED) The method of claim 8, wherein [in which] the compressed video comprises MPEG video.

11. (AMENDED) The method of claim 1, wherein [in which] information is stored identifying the paused frame, and before the

time-shifted mode occurs, [the] a predetermined frame or [the] a next frame after the predetermined frame is queued up.

13. (AMENDED) The apparatus of claim [12] 22, further comprising a real-time processing path including a real-time decoder and the time-shifted decoder that deliver real-time video to an output based on the digital video input [in which the processing paths include two decoders].

14. (AMENDED) The apparatus according to claim 13, wherein the real-time decoder and the time-shifted decoder [two decoders] are provided in a single codec.

15. (AMENDED) The apparatus of claim [12] 23, having a processing path for said real-time mode and a processing path for said time-shifted mode [in which the processing paths include an encoder and a decoder].

16. (AMENDED) The apparatus of claim [12] 21, wherein an [in which the] encoder and the time-shifted decoder [or decoders] are provided in a single codec.

17. (AMENDED) The apparatus of claim [12] 21, wherein [in which the] processing paths include buffers in [and the buffers are provided by] a common memory.

18. (AMENDED) The apparatus of claim [12] 23, wherein the [in which the video] apparatus comprises a set-top box.

19. (AMENDED) The apparatus of claim [12 in which] 23, wherein the [video] apparatus [comprises] is configured to present signals viewable by an analog television [receiver].

20. (AMENDED) A set-top box comprising:

[a compressed digital video input,

a display video output,]

a real-time decoder [coupled to the] configured to generate a first output in response to a compressed digital video input signal [and the output],

a frame storage system [coupled] configured to store said compressed digital video signal separately from said real-time decoder [the input],

a time-shifted decoder (i) coupled to the frame storage system and (ii) configured to generate a second output in response

to said stored compressed digital video signal [and the output], and

a controller [coupled to] configured to generate a command configured to control presenting (i) said first output when in a first mode and (ii) said second output when in a second mode, wherein said first output and said second output are viewable by a display device [the time-shifted decoder, the storage system, and the output].

21. (AMENDED) [An analog] A television receiver comprising:

[an uncompressed video input,

a display video output,]

a frame buffer [coupled to the input and the output,] configured to present an output in response to an uncompressed video signal,

a frame storage system configured to store said uncompressed video signal separately from said frame buffer [coupled to the input],

a time-shifted decoder configured to generate a second output in response to said stored uncompressed video signal [coupled to the output], and

a controller [coupled to] configured to generate a command configured to control presenting (i) said first output when in a first mode and (ii) said second output when in a second mode, wherein said first output and said second output are viewable by a display device [the time-shifted decoder, the storage system, and the output].

22. (AMENDED) A set-top box comprising:

[a compressed digital video input,

an uncompressed video input,

a display video output,]

a controller configured to receive a command and a compressed digital video input,

a [real-time decoder coupled to the] frame buffer configured to generate a first output in response to the compressed digital video input [and the output], and

a frame storage system coupled to the controller [input],

a time-shifted decoder coupled to the frame storage system and the controller configured to generate a second output in response to (i) said compressed digital video input, and (ii) said command; [output, and]

wherein the [a] controller [coupled to] is configured to generate a second command configured to control presenting (i) said

first output when in a first mode and (ii) said second output when in a second mode, wherein said first output and said second output are viewable by an analog display device [the time-shifted decoder, the storage system, and the output].

23. (NEW) An apparatus comprising:

a frame buffer configured to generate a first signal in response to a digital input signal;

an encoder configured to generate a second signal in response to said digital input signal, wherein said second signal is (i) stored in a buffer and (ii) retrieved separate from being stored; and

a controller configured to present an output signal comprising (i) said first signal when in a real-time mode and (ii) said retrieved second signal when in a time-shifted mode.

24. (NEW) The method according to claim 2, wherein said transition is seamless to a viewer.